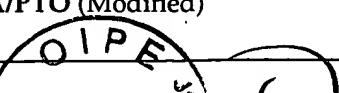


Substitute for Form 1449A/PTO (Modified)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 1 of 4 		First Named Inventor: Jin Yang	Examiner : Unassigned <i>IDS #4</i>
		Filing Date: June 30, 2000	Art Unit: 2763

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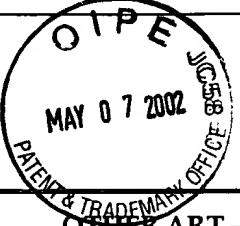
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 2 of 4 		First Named Inventor: Jin Yang	Examiner: Unassigned <i>IDS #4</i>
		Filing Date: June 30, 2000	Art Unit: 2763

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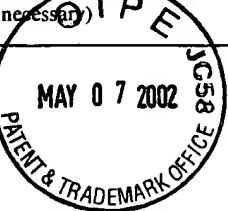
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
A <i>BS</i>		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University</i> , January 15, 1997	
B <i>EG</i>		BEREZIN, S. et al, "Model Checking Algorithms for the μ -Calculus," <i>Technical Report CMU-CS-96-180, Carnegie Mellon University</i> , September 23, 1996	
C <i>EGT</i>		BRYANT, R. E. et al, "Formal Hardware Verification by Symbolic Ternary Trajectory Evaluation," <i>28th ACM/IEEE Design Automation Conference</i> , Paper 24.2, 1991, pages 397-402	
D <i>EG</i>		BRYANT, R. E., "Binary Decision Diagrams & Beyond," Tutorial at ICCAD '95, <i>Carnegie Mellon University</i> , 1995	
E <i>EG</i>		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," <i>28th ACM/IEEE Design Automation Conference</i> , Paper 24.3, 1991, pages 403-407	
F <i>ES</i>		BURCH, J. R. et al, "Sequential Circuit Verification Using Symbolic Model Checking," <i>27th ACM/IEEE Design Automation Conference</i> , Paper 3.2, 1990, pages 46-51	
G <i>EG</i>		CAMPOS, S., "Real-Time Symbolic Model Checking for Discrete Time Models," <i>Technical Report CMU-CS-94-146, Carnegie Mellon University, Pittsburgh, PA</i> , May 2, 1994	
H <i>EC</i>		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints, <i>Computer Aided Verification, 9th International Conference, CAV '97 Proceedings (O. Grumberg, Editor)</i> , Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)	
I <i>EG</i>		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University</i> , May 1997	
J <i>EG</i>		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology</i> , Vol. 8, No. 1, January 1999, pages 49-78	
K <i>EG</i>		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design</i> , November, 1992, pages 172-178	

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 Sheet 3 of 4		First Named Inventor: Jin Yang	Examiner: 105 # 4 Unassigned
		Filing Date: June 30, 2000	Art Unit: 2763

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
L C Y		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlag, 1999	
M E Y		CLARKE, E. et al, "Another Look at LTL Model Checking," <i>Technical Report CMU-CS-94-114</i> , Carnegie Mellon University, February 23, 1994	
N E Y		CLARKE, E. et al, "Combining Symbolic Computation and Theorem Proving: Some Problems of Ramanujan," <i>Technical Report CMU-CS-94-103</i> , Carnegie Mellon University, January 1994	
O E Y		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," <i>ACM Computing Surveys</i> , Vol. 28, No. 4, December 1996, pages 626-643	
P E Y		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 343-354	
Q E Y		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
R E Y		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
S E Y		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219</i> , Carnegie Mellon University, December 1994	
T T		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	

Examiner Signature	E D GARCIA-BERRO	Date Considered	2/29/04
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 4 of 4		First Named Inventor: Jin Yang	Examiner: <i>IPS #4</i> Unassigned
		Filing Date: June 30, 2000	Art Unit: 2763

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
EJ		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
ES		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32nd ACM/IEEE Conference on Design Automation</i> , January 1995	
EL		JHA, S. et al, "Equivalence Checking Using Abstract BBDs," <i>Technical Report CMU-CS-96-187, Carnegie Mellon University, Pittsburgh, PA</i> , October 29, 1996	
EY		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
EG		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
EG		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," <i>34th Design Automation Conference</i> , June 1997	
EE		TUYA, J. et al, "Using a Symbolic Model Checker for Verify Safety Properties in SA/RT Models," <i>Proceeding of the 5h European Software Engineering Conference, Lecture Notes in Computer Science</i> , Vol. 989, Springer-Verlag, Berlin, 1995, pages 59-75	
EB		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," <i>Proceedings of Computer-Aided Verification</i> , June 1997	
ES		WING, J. M. et al, "A Case Study in Model Checking Software Systems," <i>Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA</i> , April 1996	
EY		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28th ACM/IEEE Design Automation Conference</i> , 1991	

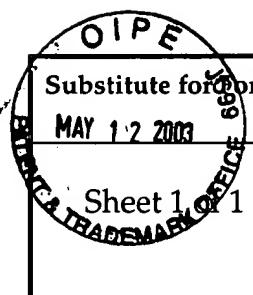
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